

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

Applicant(s): Jacobs et al.

Group Art Unit: 2183

Serial No.: 10/762,863

Confirmation No. 5930

Filed: January 22, 2004

Examiner: Vicary, Keith E.

For: COMPRESSED INSTRUCTION FORMAT FOR USE IN A VLIW
PROCESSOR

Mail Stop Appeal Brief - Patents
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

BRIEF ON APPEAL

Sir/Madam:

This brief is in furtherance of Applicants' Notice of Appeal filed on
January 25, 2010, appealing the decision of the Examiner dated October 26, 2009
rejecting claims 30-32.

I. Real Party in Interest

The real party in interest in this appeal is NXP B.V., High Tech Campus 60, 5656 AG Eindhoven, The Netherlands.

II. Related Appeals and Interferences

There are currently no related appeals or interference proceedings in progress that will directly affect, or be directly affected by, or have a bearing on the Board's decision in the present Appeal.

III. Status of Claims

Claims 1-25 were originally filed on January 22, 2004. In a preliminary amendment filed on January 22, 2004, claims 1-24 were canceled, claim 25 was amended, and new claims 26-29 were added. In response to the Office Action of January 22, 2007, claims 25-29 were canceled and new claims 30-34 were added. In response to the Office Action of October 9, 2008, claims 33 and 34 were canceled and new claims 30-32 were amended. In response to the Final Office Action of March 12, 2009, a Notice of Appeal was filed on June 11, 2009 and an Appeal Brief was filed on August 11, 2009. Claims 30-32 stand rejected in a non-final Office Action after reopening of prosecution and form the subject matter of the present appeal.

Claims 30-32 stand rejected under 35 U.S.C. 102(b) as allegedly being anticipated by U.S. Patent No. 4,251,862 ("Murayama").

This Appeal is made with regard to pending claims 30-32.

IV. Status of Amendments

No amendments were filed subsequent to the latest rejection.

V. Summary of Claimed Subject Matter

The claimed invention includes a computer storage medium (104, 103) having stored therein a sequence of instructions, which may be used in a microprocessor (101), such as a VLIW processor (See Figs. 1a and 1b, and lines 6-21 on page 7 of the Specification).

According to an embodiment, as recited in the independent claim 30, a computer storage medium (104, 103) having stored therein a sequence of instructions (See Figs. 1a and 1b, and lines 6-21 on page 7 of the Specification). The sequence of instructions includes a first instruction (INSTRUCTION 1) including a format field (FORMAT 2) that specifies an instruction compression format (See Fig. 3, and lines 1-18 on page 18 of the Specification), and a second instruction (INSTRUCTION 2), following the first instruction, that is compressed according to the format field in the first instruction (See Fig. 3, lines 1-18 on page 18, lines 16-24 on page 29, and lines 1-8 on page 30 of the Specification).

VI. Grounds of Rejection to be Reviewed on Appeal

Whether claims 30-32 are anticipated under 35 U.S.C. §102(b) by Murayama.

VII. Argument

In the Office Action of October 26, 2009, the Examiner rejected claims 30-32 under 35 U.S.C. §102(b) as allegedly being anticipated by Murayama. However, each element recited in claims 30-32 is not disclosed in the cited reference of Murayama. Thus, claims 30-32 are not anticipated under 35 U.S.C. §102(b) by Murayama.

A. Rejection of Independent Claim 30 Under 35 U.S.C. §102(b)

The independent claim 30 was rejected under 35 U.S.C. §102(b) as allegedly being anticipated by Murayama. However, the cited reference of Murayama fails to disclose each claimed element of the independent claim 30. Thus, the independent claim 30 is not anticipated by Murayama under 35 U.S.C. §102(b).

The independent claim 30 recites “*a first instruction including a format field that specifies an instruction compression format*” and “*a second instruction, following the first instruction, that is compressed according to the format field in the first instruction,*” which are not disclosed in the cited reference of Murayama. Thus, the independent claim 30 is not anticipated by the cited reference of Murayama.

A claim is anticipated only if each and every element as set forth in the claim is found, either expressly or inherently described, in a single prior art reference. *Verdegaal Bros. v. Union Oil Co. of California*, 2 USPQ2d 1051, 1053 (Fed. Cir. 1987).

In the Office Action of October 26, 2009, the Examiner alleges on pages 3 and 4 that the cited reference of Murayama discloses “a first instruction (Figure 2A, instruction k) including a format field (Figure 2, bit field 101) that specifies an instruction compression format (col. 2, lines 56-63; when the bit 101 is a “0”, field 102 is an ordinary control field, and when the bit 101 is a “1”, field 102 is used to address the sub-control memory; this further explained below); and a second instruction, following the first instruction (Figure 2A, instruction k+1), that is compressed according to the format field in the first instruction (col. 3, lines 34-39, a sub-microinstruction read out to the sub-microinstruction register 12 is activated only when the bit position 101 of the preceding main microinstruction read out from the main control memory [1] is detected to have a binary code “1” instructing the use of the sub-control memory 11; col. 5, lines 36-42, where, therefore, a microinstruction read out of the main control memory 1 includes a “1”

bit 101 instructing the use of the sub-control memory, then the preceding microinstruction is executed in the form of a large bit length comprising data read out of the main control memory 1 and data read out of the sub-control memory 11; In other words, when the bit 101 of instruction k is a “0”, an instruction k+1 is fully **compressed** in that the entire instruction is sent to the processing unit is located in the main control memory; when the bit 101 of instruction k is a “1”, an instruction k+1 is partly **compressed** into the main control memory, with the rest of the instruction located in sub-control memory)” (emphasis added). Applicants disagree with Examiner’s characterization that the instruction k+1 described in the cited reference of Murayama is compressed.

The cited reference of Murayama discloses a microprogram control system that includes in part a main control memory 1 and a sub-control memory 11, which includes microinstructions that are provided to a data-processing unit 10, as shown in Fig. 1. Main microinstructions are stored in different addresses of the main control memory 1, e.g., first and second microinstructions in addresses k and k+1, as illustrated in Fig. 2B. As explained in column 2, lines 51-56, of Murayama, each main microinstruction “shown in FIG. 2A is formed of a bit 101 instructing the use of the sub-control memory 11, a field 102 specifying one of the addresses of the sub-control memory 11 of FIG. 2B, and ordinary control fields 103, 104.” When the bit 101 of a main microinstruction is represented by a binary code “1”, then the whole field 105 of the sub-control memory 11 shown in FIG. 2B is read out upon address designation by the field 102, as explained in column 2, lines 56-60, of Murayama. As further explained in column 2, lines 66-68, and in column 3, lines 1-33, when a previous main microinstruction, e.g., the main microinstruction in address k (hereinafter “microinstruction k”), includes the bit 101 is represented by a binary code “1”, the contents of the next microinstruction, e.g., the main microinstruction in address k+1 (hereinafter “microinstruction k+1”), and the contents of the sub-control memory 11 in the address designed by the field 102 of the previous main microinstruction are delivered to the data-processing unit 10.

However, when the bit 101 of a main microinstruction is represented by a binary code “0”, then the field 102 may be applicable as an ordinary control field, as explained in column 2, lines 61-63, of Murayama. In this case, only the contents of the next main microinstruction are delivered to the data-processing unit 10. Thus, in this case, no content of the of the sub-control memory 11 is delivered to the data-processing unit 10 along with the contents of the next main microinstruction.

The Examiner alleges that the “*format field*,” as recited in the independent claim 30, is disclosed by the bit 101 described in Murayama. In addition, the Examiner alleges that the “*second instruction*,” as recited in the independent claim 30, is disclosed by the main microinstruction k+1 described in Murayama. The Examiner then asserts on page 4 of the latest Office Action that the microinstruction k+1 is either “fully compressed” or “partly compressed” into the main control memory 1, depending on the bit 101 of the main microinstruction k described in Murayama.

However, the main microinstructions in the main control memory 1, including the microinstruction k+1, are described in Murayama as being merely stored in the main control memory 1, not **compressed** into the main control memory 1. In fact, there is no mention of anything related to “compression” in Murayama. In particular, there is no mention of compressed instructions or microinstructions or any compressed data in Murayama. Applicants note herein that the relevant term “data compression” is defined in McGraw-Hill Dictionary of Scientific and Technical Terms, Sixth Edition, as “[t]he technique of reducing the number of binary digits required to represent data.” If the Examiner is asserting that mere storing of microinstructions in the main control memory 1 is equivalent to the microinstructions being compressed, Applicants respectfully assert that such interpretation is not a reasonable interpretation consistent with the specification according to the “broadest reasonable interpretation” standard, as explained in the Federal Circuit's *en banc* decision in *Phillips v. AWH Corp.*, 415 F.3d 1303, 75 USPQ2d 1321 (Fed. Cir. 2005). Thus, the microinstruction k+1

described in Murayama is not a compressed instruction. Consequently, the bit 101 is not a format field that specifies an instruction compression format. Therefore, Murayama fails to disclose “a first instruction including a format field that specifies an instruction compression format” (emphasis added) and “a second instruction, following the first instruction, that is compressed according to the format field in the first instruction” (emphasis added), as recited in the independent claim 30. Since the cited reference of Murayama fails to disclose the claimed “first instruction” and “second instruction,” the independent claim 30 is not anticipated by cited reference of Murayama.

B. Rejection of Dependent Claims 31 and 32 Under 35 U.S.C. §102(b)

Each of the dependent claims 31 and 32 depends on the independent claim 30. As such, these dependent claims include all the limitations of the independent claim 30. Thus, these dependent claims are patentable for at least the same reasons as their respective base claims.

SUMMARY

The independent claim 30 is not anticipated by Murayama under 35 U.S.C. §102(b) because Murayama fails to disclose the claimed limitation of “*a first instruction including a format field that specifies an instruction compression format*” and “*a second instruction, following the first instruction, that is compressed according to the format field in the first instruction,*” as recited in the independent claim 30. The dependent claims 31 and 32 are also not anticipated by Murayama under 35 U.S.C. §102(b) since these dependent claims include all the limitations of the independent claim 30.

For all the foregoing reasons, it is earnestly and respectfully requested that the Board of Patent Appeals and Interferences reverse the rejections of the Examiner regarding claims 30-32, so that this case may be allowed and pass to issue in a timely manner.

Respectfully submitted,
Jacobs et al.

Date: March 25, 2010

By: /thomas h. ham/
Thomas H. Ham
Registration No. 43,654
Telephone: (925) 249-1300

VIII. Claims Appendix

30. A computer storage medium having stored therein a sequence of instructions, the sequence of instructions including:

a first instruction including a format field that specifies an instruction compression format; and

a second instruction, following the first instruction, that is compressed according to the format field in the first instruction.

31. The computer storage medium of claim 30, wherein the second instruction includes a compressed operation, the compressed operation being compressed according to the first format field.

32. The computer storage medium of claim 31, wherein the second instruction includes a second format field that specifies a compression of an operation in a third instruction.

IX. Evidence Appendix

NONE

X. Related Proceedings Appendix

NONE